

**PATENT APPLICATION**

Sheet 1 of 1

<p>FORM PTO-1449</p> <p>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</p> <p>(Use several sheets if necessary)</p>	<p>ATTY. DOCKET NO. <b>200208959-1</b></p> <p>APPLICANT <b>Frederick A. Perner</b></p> <p>FILING DATE <b>herewith</b></p>	<p>APPLICATION NO. <b>10/614, 504</b></p> <p>GROUP <b>2818</b></p>	<p>CONFIRMATION NO.</p>
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**REFERENCE DESIGNATION**

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
<i>P</i>	1A	6,169,686B1	Jan. 2, 2001	Brug et al.	<i>2</i>
	1B	6,259,644B1	Jul. 10, 2001	Tran et al.	
<i>J</i>	1C	6,567,297 B2	May 20, 2003	R. Jacob Baker	
	1D	2002/0101758	Aug. 1, 2002	R. Jacob Baker	
<i>P</i>	1E	2003/0039162	Feb. 27, 2003	R. Jacob Baker	
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
<del><i>P</i></del>	1L				
<del></del>	1M				
<del></del>	1N				
<del></del>	1O				
<del></del>	1P				

**OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)**

<i>P</i>	1Q	"Nonvolatile RAM based on Magnetic Tunnel Junction Elements" by M. Durlam et al. 2000 IEEE International Solid-State Circuits Conference 07803-5853-8/00, Motorola Labs, Physical Sciences Research Labs, Tempe, AZ, Section TA 7.3
<i>P</i>	1R	"A 10ns Read and Write Non-volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell" by Roy Scheuerlein et al. 2000 IEEE International Solid-State Circuits Conference 07803-5853-8/00, IBM Research Almaden Research Center, San Jose, CA, Section TA 7.2
<i>P</i>	1S	"Offset Compensating Bit-Line Sensing Scheme for High Density DRAM's" by Yohi Watanabe et al., IEE Jurnal of Solid-State Circuits, Vol. 29, No. 1, January 1994.

EXAMINER

*Sare Auduong*

DATE CONSIDERED

*9/04*